WHAT IS CLAIMED IS:

1. A data transfer control circuit in a system large-scale integration, which controls data transfer when a plurality of bus masters access a commonly shared external device, wherein

at least one bus master of the bus masters has an arrangement for instructing pre-read of data, at the time of issuing a data read request, the data transfer control the circuit comprising:

an external address generation unit that receives an address generation instruction and generates an address signal of the external device based on an address signal issued by the one bus master;

an external device control unit that makes the external address generation unit to continuously generate an address for normal readout this time and an address for the next pre-read, upon reception of the data read request accompanied with the data pre-read instruction issued by the one bus master, and executes readout based on the next pre-read address, provided that when the normal readout this time is finished, the bus master other than the one bus master has not issued a data read request;

a data holding unit that holds the normal data read based on the normal readout address this time; and

a pre-read data storage unit that stores the pre-read data read based on the next pre-read address.

2. The data transfer control circuit according to claim 1, wherein the one bus master has an arrangement for instructing pre-read of data, respectively, with respect to a plurality of data holding areas, at the time of issuing a data read request,

the pre-read data storage unit is provided for the number of the data pre-read instructions, and

the external device control unit allows the pre-read data read by the next readout address to be held in the pre-read data storage unit corresponding to the data pre-read instruction, upon reception of the data read request from the one bus master.

3. The data transfer control circuit according to claim 1, wherein the one bus master has an arrangement for instructing a method of calculating an address of the data to be pre-read; and

the external device control unit makes the external address generation unit generate the pre-read data address using the method instructed by the one bus master.

4. The data transfer control circuit according to claim 1, wherein the data holding unit and the pre-read data storage unit are a part of a single storage unit.

5. A data transfer control circuit in a system large-scale integration, which controls data transfer when a plurality of bus masters access a commonly shared external device, comprising:

an instruction signal generation unit that generates a data pre-read instruction signal, when an address signal issued by one of the bus masters includes an address determined to be pre-read;

an external address generation unit that receives an address generation instruction and generates an address signal of the external device based on the address signal;

an external device control unit that generates the address generation instruction so that the external address generation unit continuously generates an address for performing normal readout this time and an address for performing pre-read for the next time, when the data read request issued by the one bus master is accompanied with the generation of the data pre-read instruction signal, and executes readout based on the next pre-read address, provided that bus master other than the one bus master has not issued a data read request, when the normal readout this time is finished;

a data holding unit that holds the normal data read based on the normal readout address this time; and

a pre-read data storage unit that stores the pre-read data read based on the next pre-read address.

6. The data transfer control circuit according to claim 5, wherein the data holding unit and the pre-read data storage unit are a part of a single storage unit.

7. A data transfer control circuit in a system large-scale integration, which controls data transfer when a plurality of bus masters access a commonly shared external device, comprising:

an external address generation unit that receives an address generation instruction and generates an address signal of the external device based on the address signal;

an external device control unit that generates the address generation instruction so that the external address generation unit sequentially generates a plurality of addresses for performing pre-read in addition to the address for performing the normal readout, when it judges to execute pre-read of data, upon reception of the data read request issued by the one bus master, sequentially executes readout by the pre-read addresses provided that bus master other than the one bus master has not issued a data read request, and executes readout by the normal readout address upon reception of the normal readout instruction; and

a pre-read data registration unit that registers the pre-read data read by the pre-read addresses identifiably by the address identifiers, and judges whether there is one of the address identifiers that agrees with the address in the address signal accompanying the data read request issued by the one bus master, and when there is one address that this condition, transmits the corresponding registered pre-read data to the one bus master as the readout data this time, and when there is no address that agrees this condition, generates the normal readout instruction to transmit the read normal data to the one bus master as the readout data

this time.